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Effects of Interface modification on the organic single crystal transistors have been investigated using self-assembled monolayers and double gate configurations. Systematic carrier density control associated with the shift of V_{th} was achieved by the polarized self-assembled monolayers fabricated in between the gate oxide and organic single crystals, and by the second gate electrode, which was fabricated on the other side of the primary gate electrode.

Keywords: double gate FET; interface doping; organic single crystal transistor; self-assembled monolayer

INTRODUCTION

Organic field effect transistors (OFETs) show great promise as fundamental element devices for low cost and flexible electronics such as displays, radio-frequency identification tags, and mechanical or chemical sensors. So far, rather "high-power" applications such as

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pixel control devices for active matrix flexible displays are mostly argued as promising items; however, it is not yet clear whether or not the OFETs are capable of being used for low-power devices such as logic circuits, which impose stricter requirements especially in their subthreshold regime [1]. In order to satisfy higher requirements for OFETs, various approaches are being tested, such as search for novel organic semiconductors showing high performances, search for appropriate gate dielectric and electrode materials, various device structures, and control of various interfaces which are inherent for the OFET structures.

One of the unique approaches is to use organic single crystals for the active semiconductor materials instead of polycrystalline thin films, because the surface of the single crystals are basically free from grain boundaries, which cause significant effects on the charge transport [2–4]. The single crystal OFETs show great improvements in the transistor characteristics and provide novel opportunities for fundamental study on the transport mechanisms in the organic semiconductors. Another interesting direction is the interface control, which is crucial to tune the density, injection, and trapping of carriers in the organic transistors. The most well known example is the use of self-assembled monolayers (SAMs): Putting octadecyltrichlorolsilane (OTS)-SAMs on the SiO_2 gate dielectrics improved the crystallinity of organic thin films deposited, and thus increase the field effect mobility [5].

In this paper, we report our attempts combining the use of organic single crystals and interface modifications with polar SAMs and double gate FET structures. We demonstrate that these two methods provide novel methods for fine tuning of carrier densities in the conduction channel of OFETs. Particularly, we focus on the control of the threshold voltage V_{th}, because this parameter is crucial to the design and manufacture of complicated integrated circuits. In the silicon metal-oxide-semiconductor FETs, several techniques to control V_{th} are established or even on current research; for instance changing the doping level of semiconductors and/or applying voltage bias to conductive substrates [6,7]. For the case of OFETs, on the other hand, though a pioneering work has been reported on the use of polar SAMs on thin film transistors [8], both understanding the underlying mechanism and practical applicability are still extremely primitive.

EXPERIMENTAL

Figure 1 (a) schematically shows the fabrication process of the laminated single crystal FETs. On 100–500-nm thick SiO_2/doped Si substrates, source, drain and two voltage-probing electrodes of 10-nm thick gold

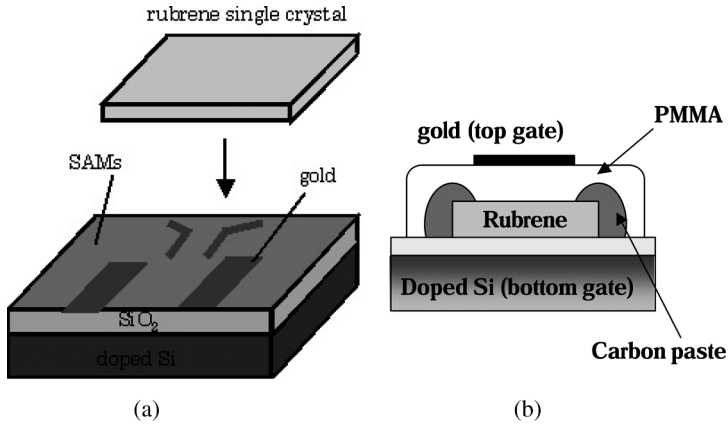

FIGURE 1 (a) A schematic of a fabrication process of single crystal OFETs. A thin platelet single crystal is gently laminated on a Si/SiO_2 substrate with a pre-patterned four terminals of gold. Organosilane- and thiol-SAMs are fabricated on SiO_2 and gold surfaces, respectively. (b) Device structure of double gate single crystal OFETs. A rubrene single crystal was placed on a surface of gate dielectric (500 nm in thickness). Source and drain electrodes were painted with carbon paste. The top gate dielectric, PMMA, was spin coated so that the thickness was about 1 μm. The top gate electrode was thermally evaporated gold.

are patterned by use of the photolithography technique. The SiO_2 gate dielectric is carefully coated with either decyltriethoxysilane or perfluorotriethoxysilane by chemical vapor deposition (CVD) technique at 150°C to form neutral CH_3-terminated SAMs (CH_3-SAMs) or electron-affine F-terminated SAMs (F-SAMs), respectively. To improve the electrical contacts between the gold pads and the molecular crystal, the substrate is treated in a solution of 10 mM nitrobenzenethiol in acetonitrile. The thiol bonds to the gold surface, so that the nitro group dopes holes into the surface of the crystal due to its large electron affinity. A thin pentacene crystal is softly placed on the substrate at the end of the process. The advantage of this method is the compatibility with the thin film devices, since the substrate preparation process is completely identical. In the case of thin film transistors, organic thin films are deposited by thermal evaporation on thus prepared substrates in place of laminating single crystals.

For the double gate experiments, we fabricated a rubrene single crystal on an unpatterned Si substrate with a gate dielectric SiO_2 with 400 nm in thickness on top of it. A thin platelet rubrene single crystal was laminated on the surface of SiO_2, followed by making source and drain electrodes with carbon paste. Then the whole surface of the

single crystal OFET device was covered by polymethylmethacrylate (PMMA), which was spin-coated with toluene solvent. On the PMMA with the thickness of about 1 μm, gold electrode for the second gate electrode was deposited by thermal evaporation. The configuration of thus fabricated double gate OFETs is described in Figure 1 (b). The measured capacitances of top and bottom gate dielectrics were 0.50 pF and 2.6 pF, respectively.

RESULTS AND DISCUSSIONS

The Effect of Polar SAMs

We plot in Figure 2 the transfer characteristics of pentacene single crystal transistors, two of which are on the CH_3-SAMs and the rest two are on the F-SAMs. The horizontal axis represents the gate voltage V_G applied to the central part in the channel, which is given by $V_G = V_{GS} + (V_1 + V_2)/2$ [9]. Hysteresis was negligible at 240 K when the gate voltage is swept back and forth in helium atmosphere. Though pronounced hysteresis appears at room temperature, introducing some ambiguity in the determination of V_{th}, the hysteresis quickly diminishes with decreasing temperature. The threshold voltage, however, remained essentially unchanged between 240 and 290 K.

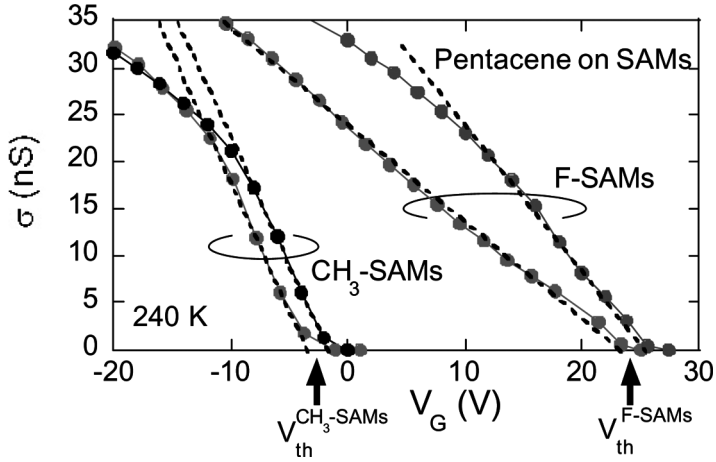

FIGURE 2 Conductance vs. gate voltage for a pentacene single crystal transistor; two samples for CH_3-SAMs, and two for F-SAMs treated devices recorded at the drain voltage of 0.5 V. The F-SAMs displays a reproducible shift of V_{th} to the positive direction, indicating an occurrence of hole accumulation. (See COLOR PLATE VI)

Obviously V_{th} differs among the two groups of pentacene single-crystal FETs; the two CH_3-SAM samples switch on at around 0 V, while the two F-SAM samples do around 25 V. The corresponding difference in the gate threshold field E_{th} is estimated to be 0.5 MV/cm, which is comparable to the value 0.7–1 MV/cm reported for polycrystalline thin-film pentacene FETs [8]. This value approximately corresponds to the carrier density of $1 \times 10^{12}\,cm^{-2}$. Noting that the present four-terminal measurements on the single crystals are free from complications such as grain boundaries and parasitic contact effects, the threshold voltage shift is an intrinsic effect at the interface between the well-ordered SAM molecules and the almost perfectly ordered pentacene molecules.

The effect of F-SAMs on the V_{th} is strongly dependent on the semiconductors. Figure 3 compares the transfer characteristics of identically prepared rubrene single crystal transistors with CH_3-SAMs and F-SAMs on 500-nm thick SiO_2 dielectrics. The two F-SAMs devices switch at the gate voltage around 4 V, while the CH_3-SAMs devices do around 0–1 V. The value of the F-SAM induced Vth shift, which corresponds to excess carrier density of $1.5 \times 10^{11}\,cm^{-2}$, is almost one order smaller than the case of pentacene single crystal (Fig. 2), and thin film transistors of pentacene and C_{60} [8]. We should also note that the experimentally observed carrier density accumulated by polar SAMs for the pentacene single crystal is more than one-order smaller than that estimated from full dipole of the isolated SAM molecule [8]. These

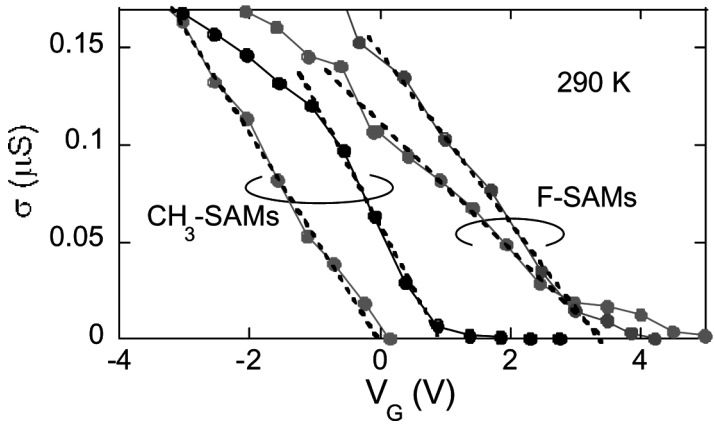

FIGURE 3 Conductance vs. gate voltage plot for a rubrene single crystal transistor at the drain voltage of 0.5 V; two samples for CH_3-SAMs, and two for F-SAMs treated devices. The V_{th} shift by the polar F-SAMs is considerably smaller than the pentacene device (Fig. 2). (See COLOR PLATE VII)

discrepancies may indicate presence of nonlocal charge redistribution in response to the moments of the SAMs. Though microscopic mechanisms are to be elucidated, the hole doping at the surface of the organic single crystals appears to be a result of self-consistent ionic-charge rearrangement in the vicinity of the interface.

The quality of the interface between the gate dielectric and semiconductor modified with SAMs manifests itself in the sharp on-off switching, particularly in CH_3-SAMs. The subthreshold swing S of the pentacene devices are around 2 V/decade. This value indicates that the interface trap density is at least comparable to or better than that of the best pentacene thin-film FETs as compared with the literature [10,11], taking into account the rather thick dielectric layer in the present devices (SCi is evaluated $\sim 14\,\mathrm{nVF/decade\,cm^2}$ as renormalized by the capacitance Ci of the gate dielectrics per area).

Double Gate Single Crystal Transistor

For a double gate transistor device, the operation was observed both in top and bottom gate voltage application, with the other gate electrode

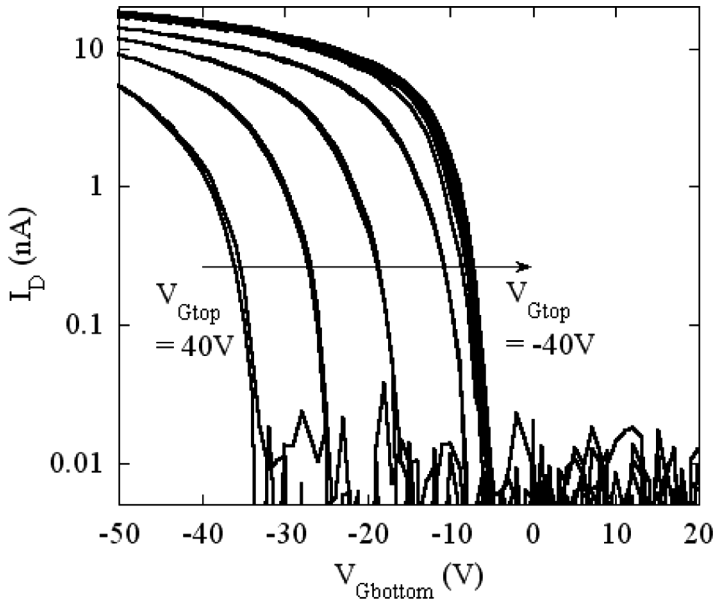

FIGURE 4 Drain current as a function of back gate voltage at the drain voltage of 5 V for different V_{Gtop} with a 10 V step. Systematic shift of V_{th} is observed by changing the top gate voltage V_{Gtop}.

floating. The field effect mobility for the top gate device was $0.04\,cm^2/Vs$, assuming that the drain current flows at the top interface between the single crystal and the PMMA gate dielectric. The mobility for the bottom gate electrodes were determined as $0.26\,cm^2/Vs$. These values are tremendously low in comparison to the top value of $20\,cm^2/Vs$ achieved in the air gap structures [12]. A possible reason for this low mobility is the unestablished processing technique, particularly in the fabrication of the top gate structure. For instance, coverage of the device with PMMA using toluene may produce damages on the rubrene single crystals. Despite these problems, we observed a typical double gate operation; modulation of a transistor operation by another gate voltage. The transfer curves for the bottom gate mode are plotted in Figure 4 for various top gate voltages V_{Gtop}. One finds that the positive V_{Gtop} continuously shifts V_{th} for the bottom gate to the negative direction, while the negative V_{Gtop} does not seriously change V_{th}. The effect of the negative V_{Gtop} is seen in the initial slope of the transfer curve: The slope shows a slight increase upon application of negative gate voltage.

The change of V_{th} and field effect mobility for the bottom gate operation is plotted as a function of V_{Gtop} in Figures 5 (a) and (b). For the

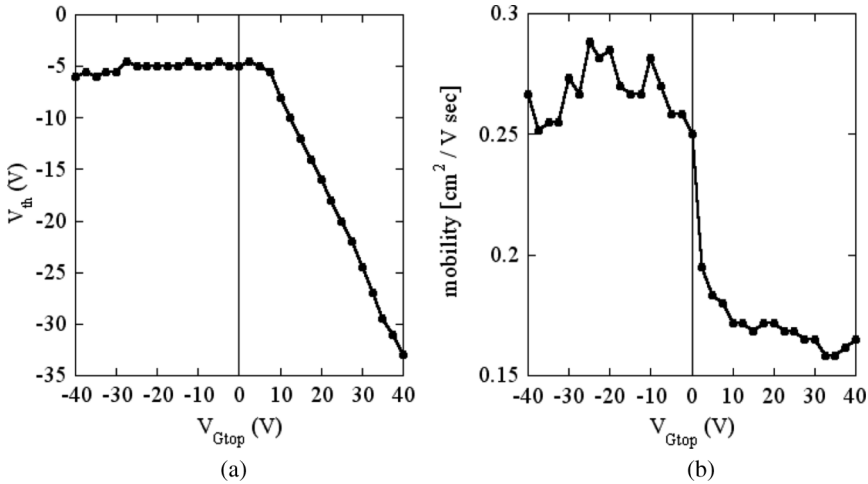

FIGURE 5 (a) V_{th} for the bottom gate operation as a function of to gate voltage V_{Gtop} derived from Figure 4. V_{th} shows a linear shift with V_{Gtop} for the positive V_{Gtop}, while it becomes independent for the negative V_{Gtop}. (b) Field effect mobility as a function of to gate voltage V_{Gtop} derived from Figure 4. Mobility shows a jump at around $V_{Gtop} = 0\,V$, possibly due to the improvement of hole injection from the drain electrode due to the charge accumulation by the top gate.

positive V_{Gtop}, V_{th} displays an approximately linear shift to the negative direction. For the negative bottom gate bias, on the other hand, V_{th} becomes more or less independent of the top gate voltage. The mobility is slightly improved by scanning V_{Gtop} from positive to negative, being suggestive of improvement of hole injection from the drain electrode to organic semiconductor, rubrene, by charge accumulation by the V_{Gtop}.

This behavior, particularly the linear shift of V_{th} against V_{Gtop}, is essentially identical to that reported for the double gate thin film transistors of pentacene [13,14]. The slope in Figure 5 (a) was approximately 0.9, which is significantly different from what is expected simply from the ratio of the measured capacitances. The flattening behavior of V_{th} at the negative V_{Gtop} region might be related to the device configurations. To improve the performance and fully understand the mechanism of single crystal double gate FETs with a considerably large thickness, we need more controlled device fabrication processes.

CONCLUSION

We have presented single crystal OFETs and their interface doping via. chemical modification with self-assembled monolayers and double gate FET device structures. Both techniques are proved to be useful for shifting V_{th} even in single crystal OFETs. In the case of polarized SAMs, we demonstrated that for pentacene, single crystal FETs show V_{th} shift with F-SAMs which are quantitatively consistent with that for the thin film FETs, indicating that the V_{th} shift by polar F-SAMs are an intrinsic phenomenon which is free from the various parasitic effects inherent to polycrystalline thin films such as grain boundaries. In the preliminary double gate transistor experiment on single crystals, we observed an essentially identical result to that for the thin film transistors, where V_{th} in the bottom gate transfer characteristics is continuously shifted by the positive top gate voltage. This is somewhat unexpected because the thickness of single crystals is comparable or larger than that for the insulator for the top gate, while this is not the case in the thin film transistors. The role of the top gate and the effect of device structures remain to be disclosed in the single crystal double gate transistors.

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